17659

21415

3 Hours / 100 Marks **Seat No.** | | | | | | | | |

Instructions : (1) All Questions are *compulsory*.

(2) Answer each next main Question on a new page.

(3) Illustrate your answers with neat sketches wherever necessary.

(4) Figures to the right indicate full marks.

Marks

1. (A) Attempt any THREE : **12**

(a) Define the terms :

(i) Metastability

(ii) Noise Margin

(iii) Power Fanout

(iv) Skew

(b) Compare BJT and CMOS. (any 4 points)

(c) State the use and syntax of :

(i) signal

(ii) variable in VHDL

(d) Compare software and hardware description languages.

(e) Write the VHDL program for 3-bit up-counter.

(B) Attempt any ONE : **6**

(a) List and explain the main steps carried in typical n-well, CMOS fabrication process with neat sketches.

(b) Describe the following statements with example :

(i) assert statement

(ii) wait statement

(iii) case statement

P.T.O.

2. Attempt any FOUR : **16**

(a) Define the terms :

(i) Oxidation

(ii) Epitaxy

(iii) Deposition

(iv) Ion-implantation

(b) State the datatypes used in VHDL.

(c) Design the following logic gates using CMOS :

(i) NOR gate

(ii) NAND gate with Truth table showing ON-OFF action.

(d) Compare concurrent and sequential statement. (Any 4 points)

(e) State and explain delta delay.

3. Attempt any FOUR : **16**

(a) Explain Moore and Mealy Machine with block diagram.

(b) Explain the process of estimation of the channel resistance and how it is calculated.

(c) Write the abbreviation of VLSI and VHDL. What is VHDL ?

(d) Design the Boolean equation using CMOS

$$Y = \overline{\overline{A + B}} + \overline{A} \cdot \overline{C}$$

(e) State and explain coding styles in VHDL :

4. (A) Attempt any THREE : **12**

(a) Explain the terms w.r.t. VHDL :

(i) Entity,

(ii) architecture (with one example)

(b) Write VHDL program to implement 4:1 Multiplexer using case statement.

(c) Draw HDL design flow for synthesis and explain.

(d) Draw internal block diagram of CPLD Xilinx series and state the function of each block.

(B) Attempt any ONE : **6**

(a) Write the VHDL program to implement 9:4 encoder.

(b) Design a sequence detector of 011 using JK flip-flop. Use mealy machine.

5. Attempt any FOUR : **16**

(a) Explain the architecture of SPARTAN-3 FPGA Family with neat diagram.

(b) Compare CPLD and FPGA. (8 points)

(c) Compare synchronous and asynchronous sequential circuit on the basis of :

(i) Definition

(ii) Clock requirement

(iii) Output affected by

(iv) Memory element

(d) List operators and their operations used in VHDL.

(e) State Event scheduling and sensitivity list.

(f) Explain : CMOS Transmission gate with diagram.

6. Attempt any FOUR : **16**

(a) Explain with neat diagram wafter processing by C-Z method.

(b) State and explain :

(i) Zero Modeling

(ii) Simulation cycle

(c) State the test bench and write its application.

(d) What is simulation ? Explain event based and cycle based simulator.

(e) Draw and explain ASIC design flow.

(f) Write the VHDL program for D-flip-flop.

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